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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,772	01/09/2002	Spiros Kalogeropulos	P-7139	7896

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EXAMINER
CHOW, CHIH CHING

ART UNIT	PAPER NUMBER
2122	

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DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/043,772	KALOGEROPULOS, SPIROS	
	Examiner	Art Unit	
	Chih-Ching Chow	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01/09/2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/07/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed on January 9, 2002.

2. The priority date considered for this application is January 9, 2002.

3. Claims 1-32 have been examined.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 5, 20 and 29 are rejected under 35 U.S.C. 112, second paragraph, claim 5 recites "the same join instructions of said join instructions after said scheduling as before said scheduling" as being indefinite in that it fails to point out what is included or excluded by the claim language. Appropriate corrections are required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1,2, 9, 13, 16, 17, 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,526,572 by Rupert Brauch et al. (hereinafter "Brauch"), in view of U.S. Patent No. 6,651,164 by (Donald Charles Soltis Jr. et al. (hereinafter "Soltis"), further in view of U.S. Patent No. 5,867,711 by Krishna Subramanian (hereinafter "Subramanian").

CLAIM	**Brauch / Soltis / Subranmanian**
1. A method comprising: (a) building a trace comprising instructions; (b) building a trace block comprising said instructions; (c) scheduling said instructions within said trace block disregarding data dependencies from any trace basic blocks, wherein at least one of said instructions is moved during said scheduling; and (d) correcting errors due to said at least one of said instructions being moved.	For claim 1 items (a) and (b), see Brauch, column 5, lines 38-41, "This **set of instructions** may be a **basic block**, superblock, **trace**, procedure, or some other **set of instructions**, depending on the design of the optimizer." For item (c), see Brauch, column 2, lines 21-25, "An operation may be beneficial if the target of the instruction is located later in the instruction window than the instruction itself, and the optimizing operation permits the mechanism to **move the instruction to an earlier point** in the instruction stream (*scheduling said instructions*)". For item (d), correcting errors actually means "to **recognize the data dependencies** from the off track blocks" (see paragraph 62 last sentence of the current application). Brauch teaches all aspects of claim 1, but he does not mention 'disregarding data dependencies' specifically, however, Soltis teaches it in an analogous prior art. In Soltis, column 1, lines 37-46, "A 'read-after-

write data dependency' exists when one instruction to be executed by a processor utilizes, during execution, data retrieved or produced from the execution of another instruction. If the one instruction executes before the other instruction executes *(disregarding dependencies)*, then an **error may occur**, since the one instruction may utilize incorrect data during execution. As a result, to **prevent errors**, steps should be taken to ensure that the instruction utilizing data retrieved or produced from the execution of another instruction does not execute until the necessary data from execution of the other instruction is available. (*correcting errors*)". Further more, Subramanian also teaches it in an analogous prior art. In Subramanian FIG. 3, it does scheduling first (*disregarding dependency*), and in FIG 4. it then does the dependency analysis.
It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to supplement Baruch's disclosure of the scheduling and data dependencies analysis by reversing the order taught by Soltis and Subramanian, for the purpose of improving the execution speed (Subramanian column 2, lines 47-48).

2. The method of Claim 1 wherein said trace comprises basic blocks comprising said instructions.

For the feature of claim 1 see claim 1 rejection. See claim 1 (a) rejection, the trace, the basic blocks comprising

'instructions'.

9. A method comprising:
(a) building a trace comprising a first basic block and a second basic block, said first basic block comprising a first instruction, said second basic block comprising a second instruction;
(b) building a trace block comprising said first instruction and said second instruction;
(c) scheduling said first instruction and said second instruction within said trace block disregarding data dependencies from off trace basic blocks, wherein said second instruction is moved from said second basic block to said first basic block during said scheduling; and
(d) correcting errors due to said second instruction being moved.

Same as claim 1 rejection, for items (a) and (b), in Brauch's disclosure, there can be multiple basic bocks, and multiple instructions; item (c) off trace block is also a basic block.

13. The method of Claim 9 further comprising building a control flow graph comprising said trace, said control flow graph further comprising an off trace basic block having an edge coming into said second basic block.

For the feature of claim 9 see claim 9 rejection. The edge works as an indicator for more basic blocks (instruction group) exist. See Soltis, FIG. 6, 112.

16. A system comprising:
(a) a processor; and
(b) a memory having a method of scheduling instructions using a trace scheduler stored therein, wherein upon execution of said method, said method comprises:
(i) building a trace comprising said instructions;

Same as claim 1 rejection.

(ii) building a trace block comprising said instructions;
(iii) scheduling said instructions within said trace block disregarding data dependencies from any off trace basic blocks, wherein at least one of said instructions is moved during said scheduling; and
(iv) correcting errors due to said at least one of said instructions being moved.

17. The system of Claim 16 wherein said trace comprises basic blocks comprising said instructions.	For the feature of claim 16 see claim 16 rejection. For rest of the features see claim 2 rejection.
24. A computer system comprising: (a) means for building a trace comprising instructions; (b) means for building a trace block comprising said instructions; (c) means for scheduling said instructions within said trace block disregarding data dependencies from any off trace basic blocks, wherein at least one of said instructions is moved during said scheduling; and (d) means for correcting errors due to said at least one of said instructions being moved.	Same as claim 1 rejection.
25. A computer program product having a method of scheduling instructions using a trace scheduler stored therein, wherein upon execution of said method, said method comprises:	Same as claim 1 rejection.

(a) building a trace comprising said instructions;
(b) building a trace block comprising said instructions;
(c) scheduling said instructions within said trace block disregarding data dependencies from any off trace basic blocks, wherein at least one of said instructions moved during said scheduling; and
(d) correcting errors due to said at least one of said instructions being moved.

26. The computer program product of Claim 25 wherein said trace comprises basic blocks comprising said instructions.	For the feature of claim 25 see claim 25 rejection. For rest of the features see claim 2 rejection.

8. Claims 3-5, 18-20, and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,526,572 by Rupert Brauch et al. (hereinafter "Brauch"), in view of U.S. Patent No. 6,651,164 by (Donald Charles Soltis Jr. et al. (hereinafter "Soltis"), further in view of U.S. Patent No. 5,867,711 by Krishna Subramanian (hereinafter "Subramanian"), and further in view of U.S. Patent No. 6,449,713 by Joel Springer Emer et al. (hereinafter "Emer").

CLAIM	Brauch/Soltis/Subranmanian/Emer
3. The method of Claim 2 wherein said building a trace block comprises: (a) adding join instructions associated with said basic blocks to said trace block; (b) appending said instructions into said trace block; and (c) mapping said instructions to said join instructions.	For the feature of claim 2 see claim 2 rejection. Brauch, Soltis, and Subramanian teach all aspects of claim 2, but he does not mention 'adding join instructions' specifically, however, Emer teaches it in an analogous prior art. For item (a), see Emer, column 6, lines 65-66, "the compiler can append a blank instruction (e.g., a NO-OP instruction)". Here the blank instructions can be treated as 'labels' like the '**join instructions**' (which is actually a NO-OP instruction). For items (b) and (c), see Emer, FIG. 5, a 'group of instructions' are moved (*appending and mapping said instructions*). It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to supplement Baruch's disclosure of the scheduling and data dependencies analysis by appending join instructions taught by Emer, for the purpose modifying instruction stream (Emer column 7, lines 2-3).
4. The method of Claim 3 wherein said correcting errors comprises remapping said instructions to said join instructions after said scheduling.	For the feature of claim 3 see claim 3 rejection. In claim 1 rejection, combining Baruch, Subranmanian and Soltis, the error corrections (after scheduling) applied to the instruction group (*remapping said instructions*).
5. The method of Claim 4 wherein said correcting errors further comprises	For the feature of claim 4 see claim 4 rejection. Error correcting would move

determining whether said instructions are mapped the same join instructions of said join instructions after said scheduling as before said scheduling.	the instructions before the scheduling to appropriate locations after the scheduling.
18. The system of Claim 17 wherein said building trace block comprises: (a) adding join instructions associated with said basic blocks to said trace block; (b) appending said instructions into said trace block; and (c) mapping said instructions to said join instructions.	For the feature of claim 17 see claim 17 rejection. For rest of the features see claim 3 rejection.
19. The system of Claim 18 wherein said correcting errors comprises remapping said instructions said join instructions after said scheduling.	For the feature of claim 18 see claim 18 rejection. For rest of the features see claim 4 rejection.
20. The system of Claim 19 wherein said correcting errors further comprises determining whether said instructions are mapped to the same join instructions of said join instructions after said scheduling as before said scheduling.	For the feature of claim 19 see claim 19 rejection. For rest of the features see claim 5 rejection.
27. The computer program product of Claim 26 wherein said building a trace block comprises: (a) adding join instructions associated with said basic blocks to said trace block; (b) appending said instructions into said trace block; and (c) mapping said instructions to said	For the feature of claim 26 see claim 26 rejection. For rest of the features see claim 3 rejection.

join instructions.

28. The computer program product of Claim 27 wherein said correcting errors comprises remapping said instructions to said join instructions after said scheduling.	For the feature of claim 27 see claim 27 rejection. For rest of the features see claim 4 rejection.
29. The computer program product of Claim 28 wherein said correcting errors further comprises determining whether said instructions are mapped to the same join instructions of said join instructions after said scheduling as before said scheduling.	For the feature of claim 28 see claim 28 rejection. For rest of the features see claim 5 rejection.

9. Claims 6, 10, 21 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,526,572 by Rupert Brauch et al. (hereinafter "Brauch"), in view of U.S. Patent No. 6,651,164 by (Donald Charles Soltis Jr. et al. (hereinafter "Soltis"), further in view of U.S. Patent No. 5,867,711 by Krishna Subramanian (hereinafter "Subramanian"), and further in view of U.S. Patent No. 6,076,159 by Rod G. Fleck et al. (hereinafter "Fleck").

CLAIM	Brauch/Soltis/Subranmanian/Fleck
6. The method of Claim 1 wherein said correcting errors comprises renaming registers of said instructions.	For the feature of claim 1 see claim 1 rejection. Brauch, Soltis, and Subranmanian teach all aspects of claim 6, but he does not mention 'register renaming' specifically, however, Fleck teaches it in an analogous prior art. In

	Fleck, column 1, lines 43-45, "Their multiple pipeline design requires, for example a dependency analysis to assure whether instructions issued in parallel are dependent on each other. Also, so called **register renaming** might be necessary if two instructions read from to the same register." It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to supplement Brauch, Soltis and Subramanian's disclosure of the scheduling and data dependencies analysis by register renaming taught by Fleck, for the purpose of parallel and multiple pipelined computer processor design (Fleck column 1, lines 24-25).
10. The method of Claim 9 wherein said correcting errors comprises renaming a register of said second instruction.	For the feature of claim 9 see claim 9 rejection. For rest of the features see claim 6 rejection.
21. The system of Claim 16 wherein said correcting errors comprises renaming registers of said instructions.	For the feature of claim 16 see claim 16 rejection. For rest of the features see claim 6 rejection.
30. The computer program product of Claim 25 wherein said correcting errors comprises renaming registers of said instructions.	For the feature of claim 25 see claim 25 rejection. For rest of the features see claim 6 rejection.

10. Claims 7, 11, 12, 22 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,526,572 by Rupert Brauch et al. (hereinafter

"Brauch"), in view of U.S. Patent No. 6,651,164 by (Donald Charles Soltis Jr. et al. (hereinafter "Soltis"), further in view of U.S. Patent No. 5,867,711 by Krishna Subramanian (hereinafter "Subramanian"), and further in view of U.S. Patent No. 6,076,159 by Rod G. Fleck et al. (hereinafter "Fleck"), and further in view of U.S. Patent No. 5,828,886 by Masakazu Hayashi et al. (hereinafter "Hayashi") .

CLAIM	Brauch / Soltis / Subranmanian / Fleck / Hayashi
7. The method of Claim 6 further comprising moving values from registers having new names registers having old names.	For the feature of claim 6 see claim 6 rejection. Brauch, Soltis, Subranmanian and Fleck teach all aspects of claim 7, but he does not mention 'moving values from registers' specifically, however, Hayashi teaches it in an analogous prior art. In Hayashi's abstract, "renames registers by replacing the register numbers used by the instructions with other register numbers according to the collected register information and the analysis of definition/referenced instruction dependency. The instructions are scheduled after the registers have been renamed." It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to supplement Brauch, Soltis and Subramanian's disclosure of the scheduling and data dependencies analysis by register renaming taught by Fleck, for the purpose of parallel and multiple pipelined computer processor design (Fleck

	column 1, lines 24-25).
11. The method of Claim 10 wherein said register renamed from an old name new name during said renaming.	For the feature of claim 10 see claim 10 rejection. For rest of the features see claim 7 rejection.
12. The method the Claim 11 wherein said correcting errors comprises inserting a move instruction into said second basic block to move a value in a register having said new name into a register having said old name.	For the feature of claim 11 see claim 11 rejection. For rest of the features see claim 7 rejection.
22. The system of Claim 21 further comprising moving values from registers having new names registers having old names.	For the feature of claim 21 see claim 21 rejection. For rest of the features see claim 7 rejection.
31. The computer program product of Claim 30 further comprising moving values from registers having new names to registers having old names.	For the feature of claim 30 see claim 30 rejection. For rest of the features see claim 7 rejection.

11. Claims 8, 14, 15, 23 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,526,572 by Rupert Brauch et al. (hereinafter "Brauch"), in view of U.S. Patent No. 6,651,164 by (Donald Charles Soltis Jr. et al. (hereinafter "Soltis"), further in view of U.S. Patent No. 5,867,711 by Krishna Subramanian (hereinafter "Subramanian"), and further in view of U.S. 2003/0079211. by Guei-Yuan Lueh (hereinafter "Lueh").

CLAIM	Brauch / Soltis / Subranmanian / Lueh
8. The method of Claim 1 wherein said correcting errors comprises adding compensation code.	For the feature of claim 1 see claim 1 rejection. Brauch, Soltis, and Subranmanian teach all aspects of claim 1, but he does not mention 'compensation code' specifically, however, Lueh teaches it in an analogous prior art. In Lueh, paragraph 26, "If no register initialization error occurred then at 406 the cloned loop which includes the register promotion transformation is executed. Upon the occurrence of exceptions e.g. ArrayIndexOutOfBound, program control is transferred to dedicated exception handlers which have been modified to include compensation code: 'a.sum=r_sum' at 408 in accordance with the invention." It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to supplement Brauch, Soltis and Subramanian's disclosure of the scheduling and data dependencies analysis by compensation code taught by Lueh, for the purpose of filling the gap between the original and the modified code.
14. The method of Claim 13 wherein said correcting errors comprises adding a compensation basic block between said off trace basic block and said second basic block.	For the feature of claim 13 see claim 13 rejection. For rest of the features see claim 8 rejection.
15. The method of Claim 14 further comprising inserting a copy of said second instruction after said renaming	For the feature of claim 14 see claim 14 rejection. For rest of the features see

second instruction after said renaming into said compensation basic block.	claim 8 rejection.
23. The system of Claim 16 wherein said correcting errors comprises adding compensation code.	For the feature of claim 16 see claim 16 rejection. For rest of the features see claim 8 rejection.
32. The computer program product of Claim 25 wherein said correcting errors comprises adding compensation code.	For the feature of claim 25 see claim 25 rejection. For rest of the features see claim 8 rejection.

Conclusion

The following summarizes the status of the claims:

35 USC § 112 (2nd) claim rejection: 5, 20, 29

35 USC § 103 claim rejection: 1-32

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chih-Ching Chow whose telephone number is 571-272-3693. The examiner can normally be reached on 7:00am - 3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chih-Ching Chow

Examiner

Art Unit 2122

CC

Chameli C. Das

CHAMELI C. DAS
PRIMARY EXAMINER

11/26/09